REMARKS

In the Office Action mailed September 7, 2006, the Examiner noted that claims 1-4, 9-13, 15-18, 23-27, 29 and 30 were pending, and rejected claims 1-4, 9-13, 15-18, 23-27, 29 and 30. Claims 1, 13, 15, 27, 29 and 30 have been amended, new claims 31 and 32 have been added. Thus, in view of the forgoing claims 1-4, 9-13, 15-18, 23-27, 29 and 30-32 remain pending for reconsideration which is requested. No new matter has been added. The Examiner's rejections are traversed below.

REJECTIONS under 35 U.S.C. § 103

Claims 13, 27 and 30 stand rejected under 35 U.S.C. § 103(a) as being obvious over Weber in view of Hauck. Weber is directed to a cache memory control architecture within a RAID storage system. Hauck is a method of retaining cache coherency in a controller. In contrast the present claims are directed to a dual cache memories accessed by a single address destination.

Independent claims 13, 27 and 30 have been amended. Support for the amendment found on page 17 line 22 through page 8 line 6 of the application. Weber and Hauck taken separately or in combination fail to reach or suggest "a master area of said one second module and a mirror area of said other second module are written to until the master area of said one second module is full, at which time said mirror area of said one first module are written," as in amended claims 13, 27 and 30.

Claims 13, 27, and 30 recite in part:

> wherein, in a case in which a capacity of a master area of said cache memory of the one second module runs short when data to be read out through said bridge module into said first module is temporarily preserved in the cache memory of the one second module, the one second module preserves the readout data in a mirror area of said cache memory of the other second module on the basis of a situation of management by said manager.

Examiner cites Hauck, Paragraph 0054-0056 as teaching the limitation. The current claims teach a method of efficiently using the cache. While Hauck discusses, a method of performing failover from one controller 720, to a replacement controller 730. With paragraph 0054 discussing which of the controllers can own particular cache lines. In contrast, the present claims discuss writing to a master area of a cache and the mirror area of a cache and only when the master area of the first cache is full starting writing in the master area of a second cache. Therefore, Hauck does not teach a "capacity of a master area of said cache memory of the one

second module runs short when data to be read out through said bridge module into said first module is temporarily preserved in the cache memory of the one second module ..."

For at least the reasons stated above, Weber and Hauck taken separately or in combination fail to teach or suggest the elements of claims 13, 27, and 30.

Claims 1-4, 9-12, 15-18, 23-26 and 29 stand rejected under 35 U.S.C. § 103(a) as being obvious over Weber in view of Hauck and Hashimoto. Hashimoto discusses an interface circuit performing data transmission between an external host controller and an external device.

Claims 1, 15 and 29 have been amended in manner similar to claims 13, 27 and 30. Hauck and Hashimoto taken separately or in combination fail to teach or suggest "a master area of said one second module and a mirror area of said other second module are written to until the master area of said one second module is full, at which time said mirror area of said one first module are written, " as in claims 1, 15 and 29.

Hashimoto paragraph 0064 states:

> With reference to FIG. 3, in the host interface circuit 103, an address generation circuit 206a is provided with two address pointers A208 and B209, and the external host controller generates two specific addresses M0 and M1 (second addresses) used for continuous access to a series of areas in the internal storage space 105 of the video coding/decoding apparatus 101 that is connected to the external host controller. The external addresses M0 and M1 correspond to the address pointers A208 and B209, respectively.

As Hashimoto discusses generation of two specific addresses used for continuous access to a series of areas, it is not writing to two mirrored cache areas. Therefore, Hashimoto does not disclose "address production means for analyzing said addressing information, which is received together with said data to be written from said first module, to produce two transferred-to addresses for designation of said two second modules having said cache memories in which said data is to be actually written and to produce written-in addresses in said cache memories," of claim 1.

For the reasons stated above, Weber, Hauck and Hashimoto do not teach or suggest the elements of claims 1, 15 and 29 and the claims dependent therefrom.

Withdrawal of the rejections is respectfully requested.

As regards dependent claims 9-12 and 23-26, nothing cited or found in Hauck suggests a master area of a cache memory. While the present claims have a mirror area, the mirror area is not analogous to the master area, and therefore, Hauck does not teach "wherein, in a case in which a capacity of a master area of said cache memory of the one second module runs short

when data to be read out through said bridge module into said first module is temporarily preserved in the cache memory of the one second module, the one second module preserves the readout data in a mirror area of said cache memory of the other second module on the basis of a situation of management by said management means," as recited in claim 9.

Weber, Hauck and Hashimoto do not teach or suggest the elements of claims 9-12 and 23-26. Withdrawal of the rejection is respectfully requested.

NEW CLAIMS

Claims 31 and 32 have been amended. Support for claims found on page 5 line 9 through page 6 line 19. The prior art as cited fails to teach or suggest "a host interface module controlling an interface to an external device, the host interface module producing an address designation; a plurality of management modules each having a cache memory, at least two of the plurality of management modules set in mirror relation to each other, a write of data to a master area of a first management module written to a mirror area of a second management module, the first management module of controlling the master area of the first management module and the mirror area of the second management module; and a bridge module connecting the host interface module and the plurality of management modules, the bridge module producing address information for two transfer to addresses of the at least two management modules of the plurality of management modules," as in claim 31.

The prior art as cited fails to teach or suggest "determining whether a master area of a first memory module is running short of space; and storing data in a mirror area of a second memory module," as in claim 32.

SUMMARY

It is submitted that the claims satisfy the requirements of 35 U.S.C. § 103. It is also submitted that claims 1-4, 9-13, 15-18, 23-27, 29 and 30-32 continue to be allowable. It is further submitted that the claims are not taught, disclosed or suggested by the prior art. The claims are therefore in a condition suitable for allowance. An early Notice of Allowance is requested.

If any further fees, other than and except for the issue fee, are necessary with respect to this paper, the U.S.P.T.O. is requested to obtain the same from deposit account number 19-3935.

Respectfully submitted,

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